IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	
Paul J. Mantey	Group Art Unit: 2111
Serial No.: 10/662,034	Examiner: Matthew D. Spittle
Filing Date: September 12, 2003	Confirmation No: 9298
For: COMMUNICATIONS BUS TRANSCEIVER	Attorney Docket No.: 200309970-1

SUPPLEMENTAL APPEAL BRIEF

To: Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the notification of non-compliant appeal brief mailed April 27, 2009, the applicants file the following supplemental appeal brief. In summary, the applicants added materials to the evidence appendix.

This brief contains items under the following headings as required by 37 CFR §41.37 and MPEP §1206:

I. Real Party In Interest
II. Related Appeals, Interferences and Judicial Proceedings
III. Status of Claims
IV. Status of Amendments
V. Summary of Claimed Subject Matter
VI. Grounds of Rejection to be Reviewed on Appeal
VII. Argument

Appendix A Claims Appendix
Appendix B Evidence Appendix
Appendix C Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC").

II. RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1-3, 6-13, and 42-44 are pending and were rejected. The rejections of claims 1-3, 6-13, and 42-44 are appealed herein. Claims 4, 5, and 14-41 have been cancelled.

IV. STATUS OF AMENDMENTS

No amendments were filed or entered subsequent to the final rejection mailed October 20, 2008.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention as claimed is summarized below with reference numerals and references to the specification and drawings. The invention is broadly set forth in the language corresponding to the below described claims. Discussions about elements of the invention can be found at least in the locations in the specification and drawings cited in the claims below.

CLAIM 1

A computer system (200) comprising:

a system bus (202) implemented in accordance with an Inter-IC bus specification; [Fig. 2A; Page 10, third through fifth paragraphs]

a bus controller (208) coupled to the system bus (202) and to a first internal bus (216);

a send machine (210) coupled between a host processor (238) and the bus controller (208) over a second internal bus (212); [Fig. 2A; page 11, third paragraph]

a first first-in first-out (FIFO) buffer (214) coupled to the send machine (210), the first FIFO (214) further coupled in parallel with the send machine (210) between the host processor (238) and the bus controller (208) over the first internal bus (216) but not over the system bus (202); [Fig. 2A; page 12, paragraphs 1 and 2]

a receive machine (222) coupled between the host processor (238) and the bus controller (208), the receive machine (222) comprising means for generation a message checksum (236i) for a message while the message is being received by the bus controller (208) over the system bus (202); [Fig. 2A; page 12, paragraph 3; page 13, paragraph 2] and

a second FIFO buffer (226) coupled to the receive machine (222) and coupled between the host processor (238) and the bus controller (208). [Fig. 2A; page 12, paragraph 4]

CLAIM 12

A computer system (200) comprising:

a system bus (202) implemented in accordance with an Inter-IC bus specification; [Fig. 2A; Page 10, third through fifth paragraphs]

a bus controller (208) coupled to the system bus (202) and to a first internal bus and a second internal bus; (216)

a send machine (210) coupled between a host processor (238) and the bus controller (208) over the second internal bus (212), the send machine (210) comprising means for transmitting the plurality of bytes over the system bus (202) without interrupting the host processor (238); [Fig. 2A; page 11, third paragraph; page 13, paragraph 1]

a first first-in first-out (FIFO) buffer (214) coupled to the send machine (210), the first FIFO (214) further coupled in parallel with the send machine (210) between the host processor (238) and the bus controller (208) over the first internal bus (216) but not over the system bus (202), the first FIFO (214) comprising means for receiving a

plurality of bytes from the host processor (238) without interrupting the host processor (238); [Fig. 2A; page 12, paragraphs 1 and 2]

a receive machine (222) coupled between the host processor (238) and the bus without interrupting the host processor (238); [Fig. 2A; page 12, paragraph 3] and

means for receiving the plurality of bytes over the system bus (202) without interrupting the host processor (238); [Fig. 2A; page 13, paragraph 1] and

means for generating a message checksum (236i) for a message while the message is being received by the bus controller (208) over the system bus (202); [Fig. 2A; page 13, paragraph 3]

a second FIFO buffer (226) coupled to the receive machine (222), the second FIFO (226) further coupled between the host processor (238) and the bus controller (208) over a third internal bus, the second FIFO (226) being coupled to the receive machine (222) over the second internal bus but not over the system bus, the second FIFO (212) buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (238). [Fig. 2A; page 12, paragraph 3, 4; page 13, paragraph 1]

CLAIM 42

A computer system (200) comprising:

a system bus (202) [Fig. 2A; Page 10, third and fourth paragraphs];

a bus controller (208) coupled to the system bus (202) and to a first internal bus (216);

a send machine (210) coupled between a host processor (238) and the bus controller (208) over a second internal bus (212), the send machine (210) comprising means for transmitting the plurality of bytes over the system bus (202) without interrupting the host processor (238) [Fig. 2A; page 11, third paragraph; page 13, paragraph 1]

a first first-in first-out (FIFO) buffer (214) coupled to the send machine (210), the first FIFO (214) further coupled in parallel with the send machine (210) between the host processor (238) and the bus controller (208) over the first internal bus (216) but not over the system bus (202), the first FIFO (214) comprising means for receiving a plurality of bytes from the host processor (238) without interrupting the host processor (238); [Fig. 2A; page 12, paragraphs 1 and 2]

a receive machine (222) coupled between the host processor (238) and the bus controller (208), the receive machine (222) comprising: [Fig. 2A; page 12, paragraph 3]

means for receiving the plurality of bytes over the system bus (202) without interrupting the host processor (238); [Fig. 2A; page 13, paragraph 1] and

means for generating a message checksum (236i) for a message with the message is being received by the bus controller (208) over the system bus (202); [Fig. 2A; page 13, paragraph 3]

a second FIFO buffer (226) coupled to the receive machine (222), the second FIFO (226) further coupled between the host processor (238) and the bus controller (208) over the second internal bus but not over the system bus, the second FIFO (226) not being coupled to the receive machine (222) over the second internal bus (212), the second FIFO buffer (226) comprising means for receiving a plurality of bytes from the bus controller (208) without interrupting the host processor (238); [Fig. 2A; page 12, paragraph 3, 4; page 13, paragraph 1]

means for receiving a message from the host processor (238); [Fig. 2A; page 13, paragraph 1]

means for attempting to send the message over the system bus (202) to a target device [Fig. 2A; page 13, paragraph 1];

means for determining whether the message was received without errors by the target device [Fig. 2A; page 13, paragraph 2];

retry means for attempting again to send the message over the system bus (202) to the target device without interrupting the host processor (238) if it is determined that

the message was not received without errors by the target device; [Fig. 2A; page 13, paragraph 3]

busfree count means (236a) for storing a busfree count associated with the computer system; [Fig. 2A; page 14, paragraph 1]

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count (236a) prior to attempting to access the system bus (202) after the system bus (202) becomes available for use; [Fig. 2A; page 14, paragraph 1]

a fair arbitration block (272) coupled between the host processor (238) and the bus controller (208), the fair arbitration block (272) comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; [Fig. 2A; page 14, paragraph 1] and

a byte timer (260) coupled between the bus controller (208) and the host processor (238), the byte timer (260) comprising means for determining whether the host processor (238) has failed and means for generating a signal indicating whether the host processor has failed (238). [Fig. 2A; page 13, paragraph 2 to page 14, paragraph 1]

CLAIM 43

A computer system (200) comprising:

a system bus (202);

a bus controller (208) coupled to the system bus (202) and to a first internal bus and a second internal bus (212);

a send machine (210) coupled between a host processor (238) and the bus controller (208) over the second internal bus (212), the send machine (210) comprising means for transmitting the plurality of bytes over the system bus (202) without interrupting the host processor (238); [Fig. 2A; page 11, third paragraph; page 13, paragraph 1]

a first first-in first-out (FIFO) buffer (214) coupled to the send machine (210), the first FIFO (214) further coupled in parallel with the send machine (210) between the host processor (238) and the bus controller (208) over the first internal bus (216) but not over the system bus (202), the first FIFO (214) comprising means for receiving a plurality of bytes from the host processor (238) without interrupting the host processor (238); [Fig. 2A; page 12, paragraphs 1 and 2]

a receive machine (222) coupled between the host processor (238) and the bus controller, the receive machine (222) comprising means for receiving the plurality of bytes over the system bus (202) without interrupting the host processor and means for generating a message checksum for a message while the message is being received by the bus controller over the system bus without interrupting the host processor (238); [Fig. 2A; page 13, paragraphs 1 and 3] and

a second FIFO (226) buffer coupled to the receive machine (222), the second FIFO (226) further coupled between the host processor (238) and the bus controller (208) over the second internal bus but not over the system bus, the second FIFO (212) not being coupled to the receive machine over the second internal bus, the second FIFO (212) buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor (238). [Fig. 2A; page 12, paragraph 3, 4; page 13, paragraph 1]

CLAIM 44

A device for use in a computer system (200) including a system bus (202) and a bus controller (208) coupled to the system bus (202) and to a first internal bus (216) and a second internal bus (212), the device comprising: [Fig. 2A; Page 10, third and fourth paragraphs]

a send machine (210) coupled between a host processor (238) and the bus controller (208) over a second internal bus (212), the send machine (210) comprising means for transmitting the plurality of bytes over the system bus (202) without

interrupting the host processor (238); [Fig. 2A; page 11, third paragraph; page 13, paragraph 1]

a first first-in first-out (FIFO) buffer (214) coupled to the send machine (210), the first FIFO (214) further coupled in parallel with the send machine (210) between the host processor (238) and the bus controller (208) over the first internal bus (216) but not over the system bus (202), the first FIFO (214) comprising means for receiving a plurality of bytes from the host processor (238) without interrupting the host processor (238); [Fig. 2A; page 12, paragraphs 1 and 2]

a receive machine (222) coupled between the host processor (238) and the bus controller (208), the receive machine (222) comprising: [Fig. 2A; page 12, paragraph 3]

means for receiving the plurality of bytes over the system bus (202) without interrupting the host processor (238); [Fig. 2A; page 13, paragraph 1] and

means for generating a message checksum (236l) for a message while the message is being received by the bus controller (208) over the system bus (202); [Fig. 2A; page 13, paragraph 3]

a second FIFO buffer (226) coupled to the receive machine (222), the first FIFO (226) further coupled between the host processor (238) and the bus controller (208) over the second internal bus but not over the system bus, the second FIFO (226) not being coupled to the receive machine (222) over the second internal bus (212), the second FIFO buffer (226) comprising means for receiving a plurality of bytes from the bus controller (208) without interrupting the host processor (238); [Fig. 2A; page 12, paragraph 3, 4; page 13, paragraph 1]

busfree count storage means for storing a busfree count (236a) associated with the computer system; [Fig. 2A; page 14, paragraph 1]

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count (236a) prior to attempting to access the system bus (202) after the system bus (202) becomes available for use; [Fig. 2A; page 14, paragraph 1] and

a fair arbitration block (272) coupled between the host processor (238) and the bus controller (208), the fair arbitration block (272) comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal. [Fig. 2A; page 14, paragraph 1]

VI. Grounds of Rejection to be Reviewed on Appeal

The appellants request that all rejections be reviewed. The grounds of rejections are as follows:

Claims 1-3 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (2003/0226050) and Yoshida (U.S. 5,928,372).

Claims 6-8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (2003/0226050) and Feeney (U.S. 6,072,781).

Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050) and Cao (5,230,044).

Claims 10 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050), Yoshida (U.S. 5,928,372), and Webb (U.S. 4,577,060).

Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050), Feeney (U.S. 6,072,781), Cao (5,230,044), and further in view of Webb (U.S. 4,577,060).

Claim 42 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050), Feeney (U.S. 6,072,781), Cao (5,230,044), Yoshida (U.S. 5,928,372), and Webb (U.S. 4,577,060).

Claim 43 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050) and Yoshida (U.S. 5,928,372).

Claim 44 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050) and Cao (U.S. 5,230,044).

VII. Argument

I Rejection of Claims 1-3 and 12 under 35 U.S.C. §103(a)

Claims 1-3 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (2003/0226050) and Yoshida (U.S. 5,928,372).

CLAIM 1

Claim 1 is printed as follows for convenience:

A computer system comprising:

a system bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the system bus and to a first internal bus:

a send machine coupled between a host processor and the bus controller over a second internal bus;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for generation a message checksum for a message while the message is being received by the bus controller over the system bus; and

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller.

Summary of Arguments

1. There is no motivation for the combination of Johnson, Yik, and Yoshida per *KSR INTERNATIONAL CO. v. TELEFLEX INC. ET AL.*, 82 U.S.P.Q.2c 1385, (U.S. 2007).

Arguments

KSR

The Supreme Court in KSR stated "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." Id at 1396. The applicant holds that the final office action has no rational underpinning with regard to the combination. More specifically, the applicant contends that the combination combines elements of different references in such a way that the final product would not work. Therefore, the combination lacks articulated reasoning and has no rational underpinning.

Johnson/Yik Combination

With regard to the element of a send machine, the office action states that Johnson teaches a send machine as element 707 of Fig. 7, which is a message data register. Fig. 7 is attached hereto for convenience as attachment 1. The office action acknowledges that Johnson fails to teach that the send machine and the FIFO buffer are connected as recited in claim 1.

The applicant contends that at this point, the suggested combination starts to lose rational underpinning. The office action states that Yik teaches circuits that may be implemented in Johnson in place of elements 514 and 516 of Johnson in order to constitute the recited send machine. More specifically, the office action states that the bridge (reference numeral 100 of Fig. 1 of Yik) could be implemented in place of elements 514 and 516 of Johnson. For convenience, Fig. 1 of Yik is attached as attachment 2.

The applicant contends that the combination of Johnson and Yik, as suggested by the office action, does not work and is without rational underpinnings. The most obvious problem with the suggested combination is that the bridge 100 of Yik has several lines connected to the frame processor 102. These lines do not exist between the elements 514, 515 and the system interface processor 312 of Johnson. Thus, Johnson would have to be further modified to enable the processor 312 to operate the bridge 100 of Yik. There is no suggestion in the office action as to how this would work and the applicant is not aware of how this would work. Thus, the combination cannot be obvious.

On page 3 of the office action, it is stated that the combination of Yik and Johnson teach a send machine (Yik 150) coupled between a host processor (Johnson 200) and the bus controller (Johnson 312). It is noted that the "send machine" 150 is a component of the bridge 100 of Yik, that was located in place of elements 514 and 516 of Johnson. The problem here is that Johnson includes the MDR 707 as shown in attachment 1, which the office action states is the send machine of claim 1. Thus, according to the office action, Johnson has a first send machine, which is the MDR 707, and a second send machine which is within the bridge 100 of Yik that is put in place of the elements 514 and 516. Therefore, if Yik provides the send machine 150, it will be located between the system interface 312 of Johnson and the other send machine 707 of Johnson and not a bus as claimed. Based on the foregoing, this combination does not render the elements of claim 1 and cannot render claim 1 obvious.

Between pages 3 and 4 of the final office action, it is stated that Yik teaches a receive machine and FIFO as elements 136 and 142. The "receive machine" of Yik is associated with a bus 144 and the FIFO is associated with a bus 146. The second paragraph of page 4 of the final office action states that the combination of Yik and Johnson is obvious.

When the results of the combination are analyzed, it is apparent that the combination is not obvious and has no rational underpinning. Johnson (Fig. 7) shows a single data line extending between a system interface processor 312 and an ISA bus 226. In order to add Yik to Johnson, the queues 514 and 516 are replaced with the bridge 100 of Yik. According to the office action, the addition of Yik into Johnson provides the claimed send machine, receive machine, and their FIFOs. However, Johnson still has the MDR 707, which, according to the final office action is a send machine. Now there are two send machines, which conflicts with claim 1.

Another problem with the combination is the number of bus lines. Johnson has been designed with the single data line shown in Figs. 4 and 7. Yik, however, requires four data lines, 144, 146, 156, and 158. These additional data lines further require changes to the system interface processor 312, the ISA bus 226, and the CPUs 200. There is no rational underpinning for these modifications to Johnson. Therefore, the applicant contends that the combination is not obvious.

Addition of Yoshida

The final office action acknowledges that the combination of Johnson and Yik does not provide the checksum element of claim 1. In order to overcome this deficiency, the office action states that it would be obvious to add the check sum of Yoshida to the above combination. There is no mention in the final office action as to how Yoshida could be incorporated into the Johnson/Yik combination and it is not apparent to the applicant. Therefore, the applicant contends that the combination is not obvious as it is not articulated and lacks rational underpinning.

Conclusion

Based on the foregoing, there is no rational underpinning for the Johnson/Yik/Yoshida combination. Rather, the applicant contends that the combination is a piecemeal of different devices that would not function if combined as suggested by the final office action Thus, the combination is not obvious and the applicant requests reversal of the rejection in the final office action.

CLAIMS 2, 3, and 12

Claims 2, 3, and 12 were rejected based on the same combination as claim 1. As stated above, the Johnson/Yik/Yoshida combination is not proper. Therefore, claims 2, 3, and 12 will stand or fall with claim 1 solely for the purposes of this appeal.

II. Rejection of Claims 6-8 Under 35 U.S.C. §103(a)

Claims 6-8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (2003/0226050) and Feeney (U.S. 6,072,781). Claims 6-8 are dependent on claim 1 and will stand or fall with claim 1 solely for the purposes of this appeal.

III. Rejection of Claim 9 Under 35 U.S.C. §103(a)

Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050) and Cao (5,230,044). Claim 9 is dependent on claim 1 and will stand or fall with claim 1 solely for the purposes of this appeal.

IV. Rejection of Claims 10 and 11 Under 35 U.S.C. §103(a)

Claims 10 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050) and Webb (U.S. 4,577,060). Claims 10 and 11 are dependent on claim 1 and will stand or fall with claim 1 solely for the purposes of this appeal.

V. Rejection of Claim 13 Under 35 U.S.C. §103(a)

Claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050), Feeney (U.S. 6,072,781), Cao (5,230,044), and further in view of Webb (U.S. 4,577,060). Claim 13 will stand or fall with claim 12 solely for the purposes of this appeal.

VI. Rejection of Claim 42 Under 35 U.S.C. §103(a)

Claim 42 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050), Feeney (U.S. 6,072,781), Cao (5,230,044), Yoshida (U.S. 5,928,372), and Webb (U.S. 4,577,060).

As with claims 1 and 12, the applicant argues that the Johnson/Yik/Feeney/Cao/Yoshida/Webb combination is improper. More specifically, the applicant contends that the combination of these six references lacks rational underpinning as required by KSR. In addition, the applicant asks the question that if claim 42 is obvious, why does it take six references to render claim 42 obvious?

Johnson and Yik

The office action states that the aforementioned combination of Johnson and Yik teach the bus controller, the send machine, the receive machine, and the FIFOs as set forth in claim 1. As stated in the rebuttal to the rejection of claim 1, this combination does not work. More specifically, applying Yik into Johnson as stated by the office action does not yield the elements of claim 1 and will not work.

Yoshida

Page 16 of the office action states that Yoshida teaches a checksum. The applicant notes that a checksum is not necessarily recited in claim 42. However, as stated above in the rebuttal to the rejection of claim 1, Yoshida cannot be combined with Johnson and Yik. In addition, the office action does not disclose how Yoshida is to be combined with Johnson and Yik.

Feeney

The office action relies on Feeney to teach the retry means. In other words, Feeney has to be incorporated into the Johnson/Yik/Yoshida combination because neither Johnson, nor Yik, nor Yoshida teach a retry means. The applicant notes that the office action does not indicate how Feeney is to be implemented into the Johnson/Yik/Yoshida combination. For example, the processor in Johnson will have to be changed in order to communicate with the send machine in Yik and with the other send machine 707 of Johnson. Had this been obvious, it seems that Yik or Johnson would have implemented it. Furthermore, the check sum of Yoshida has to be implemented with the retry means of Feeney. Again, if this is obvious, why wasn't it disclosed in Yoshida.

Cao

Page 18 of the office action states that Cao teaches the bus free count means, the busfree timer, and the fair arbitration block. Thus, we have to add the fifth reference, Cao, into the Johnson/Yik/Yoshida/Feeney combination such that the device works and is obvious. The fair arbitration block element of claim 42 recites the following:

> **a fair arbitration block coupled between the host processor and the bus controller**, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal
> (emphasis added)

In order for Cao to be added to the Johnson/Yik/Yoshida/Feeney combination, any bus free or arbitration existing in any reference needs to be replaced by Cao. There is no indication in the office action as to how this addition of Cao to the previous combination can be accomplished.

In addition, the fair arbitration block element of claim 42 requires that the fair arbitration block be coupled between the host processor and the bus controller. There is no indication of this limitation in Cao. Likewise, the fair arbitration element requires a priority signal. There is no description in the office action as to where this priority signal is located and the applicant does not know where it is located in Cao.

Therefore, even if it is practical to incorporate Cho into the Johnson/Yik/Yoshida/Feeney combination, the arbitration block taught by Cao does not teach the arbitration block of claim 42. Therefore, the fair arbitration block of claim 42 is not rendered obvious by the combination.

Webb

The office action relies on Webb to teach the byte timer of element of claim 42. Therefore, Webb has to be incorporated into the Johnson/Yik/Yoshida/Cao/Feeney combination in order to yield claim 42 obvious. The byte timer element of claim 42 recites the following:

> **a byte timer coupled between the bus controller and the host processor**, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.
> (emphasis added)

The is no indication how Webb is to be implemented between the bus controller and the host processor, especially in light of all the previous modifications that have been required for Johnson and Yik. Thus, the addition of Webb does not yield claim 42 obvious.

Based on the foregoing, the combination of Johnson, Yik, Yoshida, Cao, Feeney, and Webb does not have any rational underpinnings and does not render claim 42 obvious.

IV. Rejection of Claim 43 Under 35 U.S.C. §103(a)

Claim 43 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050) and Yoshida (U.S. 5,928,372).

As stated above in the rebuttal to the rejection of claim 1, the combination of Johnson and Yik lack rational underpinnings. Therefore, claim 43 will stand or fall with claim 1 solely for the purposes of this appeal.

V. Rejection of Claim 44 Under 35 U.S.C. §103(a)

Claim 44 was rejected under 35 U.S.C. §103(a) as being unpatentable over Johnson (U.S. 6,122,758) in view of Yik (U.S. 2003/0226050), Yoshida (U.S. 5,928,372), and Cao (U.S. 5,230,044).

As stated above in the rebuttal to the rejection of claim 1, the combination of Johnson and Yik lack rational underpinnings. Therefore, claim 44 will stand or fall with claim 1 solely for the purposes of this appeal.

In view of the above, all of the claims are believed to be in condition for allowance, and the Applicant respectfully requests that the rejections be overturned.

Respectfully submitted,
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Claim 1 (previously presented). A computer system comprising:

a system bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the system bus and to a first internal bus:

a send machine coupled between a host processor and the bus controller over a second internal bus;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for generation a message checksum for a message while the message is being received by the bus controller over the system bus; and

a second FIFO buffer coupled to the receive machine and coupled between the host processor and the bus controller.

Claim 2 (original). The computer system of claim 1, wherein the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor without interrupting the host processor.

Claim 3 (previously presented). The computer system of claim 1, wherein:

the first FIFO buffer comprises means for receiving a plurality of bytes from the host processor; and

the send machine comprises means for transmitting the plurality of bytes over the system bus without interrupting the host processor.

Claim 4 (canceled).

Claim 5 (canceled).

Claim 6 (previously presented). The computer system of claim 1,

further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device; and

retry means for attempting again to send the message over the system bus to the target device if it is determined that the message was not received without errors by the target device.

Claim 7 (previously presented). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device.

Claim 8 (previously presented). The computer system of claim 6, wherein the retry means comprises means for attempting again to send the message over the system bus to the target device without obtaining the message again from the host processor if it is determined that the message was not received without errors by the target device.

Claim 9 (previously presented). The computer system of claim 1, further comprising:

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

Claim 10 (original). The computer system of claim 1, further comprising:

a byte timer coupled between the bus controller and the host processor.

Claim 11 (previously presented). The computer system of claim 10, wherein the byte timer comprises means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 12 (previously presented). A computer system comprising:

a system bus implemented in accordance with an Inter-IC bus specification;

a bus controller coupled to the system bus and to a first internal bus and a second internal bus;

a send machine coupled between a host processor and the bus controller over the second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus without interrupting the host processor; and

means for receiving the plurality of bytes over the system bus without interrupting the host processor; and

means for generating a message checksum for a message while the message is being received by the bus controller over the system bus;

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over a third internal bus, the second FIFO being coupled to the receive machine over the second internal bus but not over the system bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

Claim 13 (previously presented). The computer system of claim 12, further comprising:

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claims 14-41 (canceled) .

Claim 42 (previously presented). A computer system comprising:

a system bus;

a bus controller coupled to the system bus and to a first internal bus;

a send machine coupled between a host processor and the bus controller over a second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising:

means for receiving the plurality of bytes over the system bus without interrupting the host processor; and

means for generating a message checksum for a message with the message is being received by the bus controller over the system bus;

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

means for receiving a message from the host processor;

means for attempting to send the message over the system bus to a target device;

means for determining whether the message was received without errors by the target device;

retry means for attempting again to send the message over the system bus to the target device without interrupting the host processor if it is determined that the message was not received without errors by the target device;

busfree count means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use;

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal; and

a byte timer coupled between the bus controller and the host processor, the byte timer comprising means for determining whether the host processor has failed and means for generating a signal indicating whether the host processor has failed.

Claim 43 (previously presented). A computer system comprising:

a system bus;

a bus controller coupled to the system bus and to a first internal bus and a second internal bus;

a send machine coupled between a host processor and the bus controller over the second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising means for receiving the plurality of bytes over the system bus without interrupting the host processor and means for generating a message checksum for a message while the message is being received by the bus controller over the system bus without interrupting the host processor; and

a second FIFO buffer coupled to the receive machine, the second FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor.

Claim 44 (currently amended). A device for use in a computer system including a system bus and a bus controller coupled to the system bus and to a first internal bus and a second internal bus, the device comprising:

a send machine coupled between a host processor and the bus controller over a second internal bus, the send machine comprising means for transmitting the plurality of bytes over the system bus without interrupting the host processor;

a first first-in first-out (FIFO) buffer coupled to the send machine, the first FIFO further coupled in parallel with the send machine between the host processor and the bus controller over the first internal bus but not over the system bus, the first FIFO comprising means for receiving a plurality of bytes from the host processor without interrupting the host processor;

a receive machine coupled between the host processor and the bus controller, the receive machine comprising:

means for receiving the plurality of bytes over the system bus without interrupting the host processor; and

means for generating a message checksum for a message while the message is being received by the bus controller over the system bus;

a second FIFO buffer coupled to the receive machine, the first FIFO further coupled between the host processor and the bus controller over the second internal bus but not over the system bus, the second FIFO not being coupled to the receive machine over the second internal bus, the second FIFO buffer comprising means for receiving a plurality of bytes from the bus controller without interrupting the host processor;

busfree count storage means for storing a busfree count associated with the computer system;

a busfree timer for use by the computer system to wait an amount of time specified by the busfree count prior to attempting to access the system bus after the system bus becomes available for use; and

a fair arbitration block coupled between the host processor and the bus controller, the fair arbitration block comprising arbitration means for modifying the busfree count according to a priority signal to produce an arbitrated busfree count signal.

Appendix B Evidence Appendix

Attachment 1 is Fig. 7 of Johnson.

Attachment 2 is Fig. 1 of Yik.

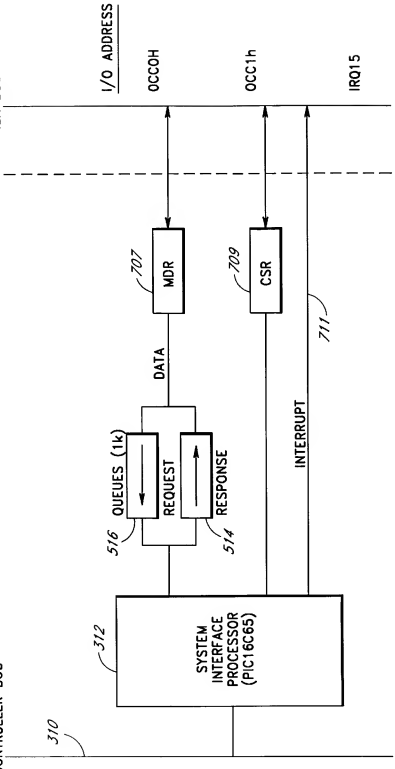
MICRO CONTROLLER BUS
310
ISA TO MICROCONTROLLER BUS INTERFACE
312
SYSTEM INTERFACE PROCESSOR (PIC16C65)
516
QUEUES (1k)
REQUEST
514
RESPONSE
DATA
707
MDR
709
CSR
INTERRUPT
711
ISA BUS
226
I/O ADDRESS
OCC0H
OCC1h
IRQ15

FIG. 7

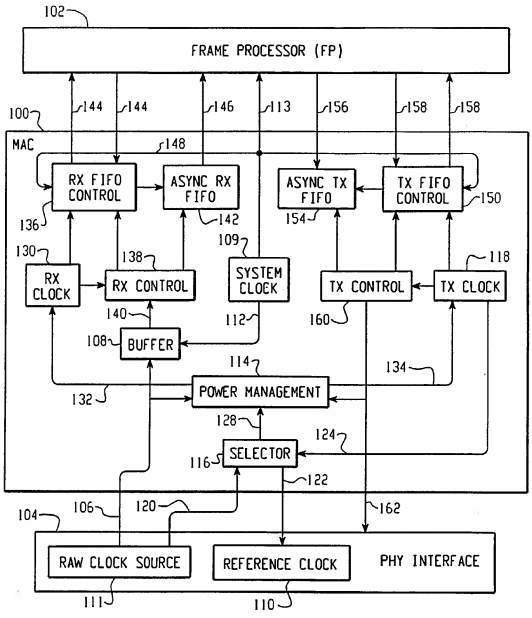
102
FRAME PROCESSOR (FP)
100
144
144
146
113
156
158
158
MAC
148
RX FIFO CONTROL
ASYNC RX FIFO
ASYNC TX FIFO
TX FIFO CONTROL
150
136
142
154
109
130
138
118
RX CLOCK
RX CONTROL
SYSTEM CLOCK
TX CONTROL
TX CLOCK
140
112
160
108
BUFFER
114
134
132
POWER MANAGEMENT
128
124
116
SELECTOR
122
104
106
120
162
RAW CLOCK SOURCE
REFERENCE CLOCK
PHY INTERFACE
111
110

Fig. 1

Appendix C Related Proceedings Appendix

None